



2116

PTO/SB/21 (08-03)

# TRANSMITTAL FORM

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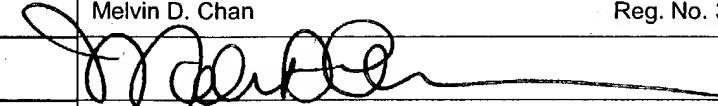
Application Number	09/880,734
Filing Date	June 12, 2001
First Named Inventor	Crosland, Andrew
Art Unit	2116
Examiner Name	Tse W. Chen
	RECEIVED MAY 10 2004 Technology Center 2100

Attorney Docket Number 15114-053500US

## ENCLOSURES (Check all that apply)

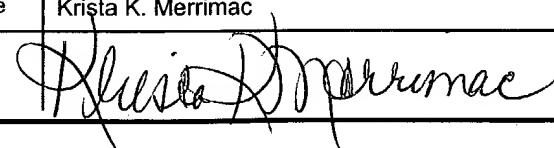
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached  <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s)  <input type="checkbox"/> Extension of Time Request  <input type="checkbox"/> Express Abandonment Request  <input checked="" type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s)  <input type="checkbox"/> Response to Missing Parts/ Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer  <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s)	<input type="checkbox"/> After Allowance Communication to Group <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter  <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below):
		Remarks
The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.		

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual	Townsend and Townsend and Crew LLP Melvin D. Chan	
Signature		
Date	Reg. No. 39,626 May 5, 2004	

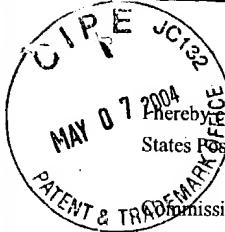
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By:

**PATENT**  
Attorney Docket No.: 15114-053500US  
Client Reference No.: A618

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MAY 10 2004

Technology Center 2100

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

ANDREW CROSLAND et al.

Application No.: 09/880,734

Filed: June 12, 2001

For: EMBEDDED PROCESSOR WITH  
WATCHDOG TIMER FOR  
PROGRAMMABLE LOGIC

Examiner: Tse W. Chen

Art Unit: 2116

**SUPPLEMENTAL INFORMATION  
DISCLOSURE STATEMENT UNDER 37  
CFR §1.97 and §1.98**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

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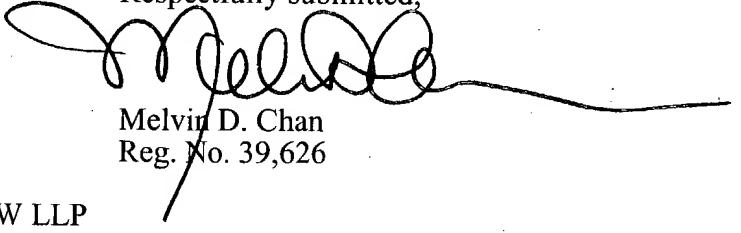
ANDREW CROSLAND et al.  
Application No.: 09/880,734  
Page 2

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Applicant believes that no fee is required for submission of this statement.

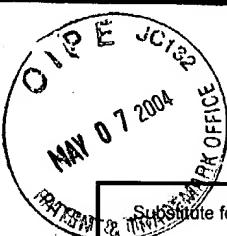
However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

  
Melvin D. Chan  
Reg. No. 39,626

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Substitute for form 1449A/PTO				<b>Complete if Known</b>	
				Application Number	09/880,734
				Filing Date	June 12, 2001
				First Named Inventor	Crosland, Andrew
				Art Unit	2116
				Examiner Name	Tse W. Chen
Sheet	1	of	2	Attorney Docket Number	15114-053500US

<b>U.S. PATENT DOCUMENTS+</b>					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number Number Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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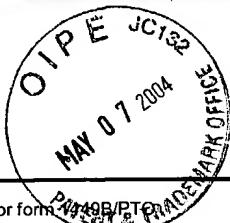
<b>FOREIGN PATENT DOCUMENTS</b>						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Sheet <b>2</b>		of <b>2</b>	Application Number <b>09/880,734</b> Filing Date <b>June 12, 2001</b> First Named Inventor <b>Crosland, Andrew</b> Art Unit <b>2116</b> Examiner Name <b>Tse W. Chen</b> Attorney Docket Number <b>15114-053500US</b>		

<b>NON PATENT LITERATURE DOCUMENTS</b>				
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T <sup>2</sup>
	AO	DeHON, DPGA-Coupled Microprocessors: Commodity ICs for the Early 21st Century, Artificial Intelligence Laboratory, Massachusetts Institute of Technology, Cambridge, MA, IEEE, February, 1994, pp. 31-33		
	AP	HAUSER, and WAWRZYNEK, University of California, Berkeley, "Garp: A MIPS Processor with a Reconfigurable Coprocessor," IEEE, April 1997, pp. 12-21.		
	AQ	IBM Corporation, "Mixture of Field and Factory Programmed Logic Cells in a Single Device," IBM Technical Disclosure Bulletin, April 1995, pp. 499-500		
	AR	NAGEL, "ACM Computing Surveys: Synergy Between Software and Hardware," Carnegie Mellon University, Department of Electrical Engineering and Computer Science, Pittsburgh, PA, December, 1996, pp. 1-3.		
	AS	RAZDAN, and SMITH, "A High-Performance Microarchitecture with Hardware-Programmable Functional Units," Harvard University, Cambridge, MA, Digital Equipment Corporation, Hudson, MA, November, 1994, pp. 172-180.		
	AT	WITTIG, and CHOW, "OneChip" An FPGA Processor With Reconfigurable Logic, Department of Electrical and Computer Engineering, University of Toronto, Ontario, Canada, IEEE, September, 1996, pp. 126-135.		
	AU	WYNN, "In-Circuit Emulation for ASIC-Based Designs," Xilinx, Inc., VLSI Systems Design, October, 1986, pp. 38-39, and 42-45.		
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